(19) Japanese Patent Office (JP)

(12) Publication of Laid-Open Patent Application (A)

(11) Publication Number of Patent Application:

Japanese Patent Laid-Open Publication No.Hei3-141391

(43) Date of Publication: June 17,1991(Heisei 3)

(51) Int.Cl.[5] G 09 G 3/36 G02 F 1/133 G 09 G 3/20

Identification Mark: 505 J

JPO file number 8621-5C 7709-2H 8621-5C

Request for Substantive Examination: Not requested

Number of Claims: 2 (8 pages in total)

---

(54) Title of the Invention: Multi-output driver integrated circuit

(21) Application Number: Japanese Patent Application No. Hei1-280388

(22) Date of Filing: October 27, 1989 (Hei1)

(72) Inventor: Sadamichi TOI

c/o Fuji Electric Co., Ltd.

1-1, Tanabeshinden, Kawasaki-ku, Kawasaki-shi, Kanagawa

(71)Applicant: Fuji Electric Co., Ltd.

1-1, Tanabeshinden, Kawasaki-ku, Kawasaki-shi, Kanagawa

(74)Agent: Patent attorney Minoru YAMADA

Description

1. Title of the Invention

Multi-output driver integrated circuit

2. Scope of Claims

(1) A multi-output driver integrated circuit comprising n switching means each of which is provided corresponding to each load, characterized in that:

the each switching means comprises m switching circuits which are connected in parallel;

the m switching circuits share a common control signal and an output terminal; and

the each switching circuit comprises a switching element for charge to charge from a power source side to a load side and a switching element for discharge to discharge the charge amount to a ground side, which are switched on/off exclusively from each other by the common control signal, and comprises a switching element for selecting a charge element to conduct/disconnect between the power source side and the switching element for charge and a switching element for selecting a discharge element to conduct/disconnect between the switching element for discharge and the ground side, which are switched on/off by a selecting control signal.

(2) A multi-output driver integrated circuit comprising n switching means each of which is provided corresponding to each load, characterized in that:

the each switching means comprises m switching circuits which are connected in parallel;

the m switching circuits share a common control signal and an output terminal; and

the each switching circuit comprises a switching element for charge to charge from a power source side to a load side and a switching element for discharge to discharge the charge amount to a ground side, which are switched on/off exclusively from each other by the common control signal, and comprises a switching element for selecting a charge element, which is switched on/off by a dedicated charge selecting control signal to conduct/disconnect between the power source side and the switching element for selecting a discharge element, which is switched on/off by a dedicated discharge selecting control signal.

3. Detailed Description of the Invention

[Industrial field of the Invention]

The present invention relates to a multi-output driver integrated circuit which drives a number of LCDs (liquid crystal display elements) or the like, and especially relates to a multi-output driver integrated circuit which is capable of varying and controlling on-resistance and on/off response speed (transmission time) for each output.

[Prior Art]

As shown in FIG. 11, a conventional LCD driver integrated circuit comprises a shift register 1 with n stages (for example a 64-bit) in which a serial data signal DIN is shifted to the next stage when a transfer clock CLK is inputted, a latch circuit array portion 2 in which a content of the each stage of the shift register 1 is taken as parallel data in synchronization with an input of a latch signal LATCH and temporarily stored, a data selection portion 3 in which output portion control signals IN_1 to IN_{64} are generated based on an output of the each latch circuit and a condition input (an enable signal and the like), and an output transistor array portion 4 which charges and discharges each

LCDs (loads) connected to output terminal OUT_1 to OUT_{64} based on the respective output portion control signals IN_1 to IN_{64}.

As each of output transistor portions 4_1 to 4_{64} of the transistor array portion 4, for example, there is known configurations shown in FIG. 12(A) and (B). The output transistor portion shown in FIG. 12 (A) is a CMOS inverter circuit which comprises an N-Channel MOSFET 5 for charge and a P-Channel MOSFET 6 for discharge which switch on/off exclusively from each other by the output portion control signal, and is applied to a low voltage driver using a logic circuit power source V_{DD}. Note that an LCD comprises a load resistor R_L and a load capacitor C_L equivalently as a load L. The output transistor portion shown in FIG. 12(B) is applied to a high voltage driver using a high voltage power source V_H, which is provided with a level shift function for step-up converting a logic circuit power source voltage to a high voltage power source voltage for driving an LCD, and comprises a P-Channel MOSFET 7 which is connected with voltage dividing resistors R_1, R_2, and a resistor R_3 in series and is switched on/off by an output portion control signal IN_i and a high withstand-voltage MOSFET 8 for charge and a high withstand-voltage MOSFET 9 for discharge which are gate-driven exclusively from each other by switching on/off of the P-channel MOSFET 7.

[Problems to be solved by the Invention]

However, in such a multi-output driver integrated circuit, there are variations in loads between LCDs serving as elements to be driven, and characteristic variations are inevitably generated between output transistor portions. Therefore, variations in signal transmission time (response time) and in on-resistance are generated for each output. That is, as shown in FIG. 13 for example, when the transmission time between falling of

the latch signal LATCH and rising of the output OUT 1 in the output transistor portion 4_2 is TPD 1, an on-voltage is 100V, and if these are set as standard values, the transmission time TPD 2 of the output OUT 2 in the output transistor portion 4_2 is longer than that of the output OUT 1, and an on-voltage of the output OUT 2 is 99V which is lower than that of the output OUT 1.

Accordingly, the present invention is to solve the above-mentioned problems, and the object is to provide a multi-output driver integrated circuit which can correct the variations of the transmission time and the on-voltage of for each output by adopting a method for varying and controlling each output increasingly or decreasingly.

[Means to solve the problems]

To solve the above-mentioned problems, in a multi-output driver integrated circuit having n switching means each of which is provided corresponding to each load, the means which is taken in the present invention comprises m switching circuits in which the above-mentioned switching means are connected in parallel, and the m switching circuits share a common control signal and an output terminal. As the each of the switching circuit, it comprises a switching element for charge to charge from a power source side to a load side and a switching element for discharge to discharge the charge amount to a ground side, which are switched on/off exclusively from each other by the common control signal, and a switching element for selecting a charge element to conduct/disconnect between a power source side and the switching element for charge and an element for selecting a discharge element to conduct/disconnect between the switching element for discharge and a ground side which are switched on/off exclusively from each other by the selecting control signal In addition, the another

means is that the switching element for selecting a charge element and the switching element for selecting a discharge element are individually controlled by a dedicated charge selecting control signal, and a dedicated discharge selecting control signal respectively.

[Operation]

According to such a means, each switching means does not charge or discharge by a single control signal primarily, and only a switching circuit preferentially selected from m switching circuits which constitute the switching means by a selecting control signal charges or discharges by a common control signal. Therefore, as for a switching means, it is possible to vary and control an on-voltage by selecting a predefined number of these from among the m switching circuits by a selecting control signal programmatically. When the number of switching circuits selected in a particular switching means is large, since these are connected in parallel, the on-resistance becomes low, and the voltage drop becomes low. Thus, the on-voltage becomes high. In addition, as the on-resistance becomes low, and the rising property becomes steep, and the transmission time becomes short as a result. Therefore, it is possible to correct the variation of the on-voltage and the transmission time between each output.

However, since the switching element for selecting a charge element and the switching element for selecting a discharge element in the each switching circuit are selected by the selecting control signal simultaneously, if the rising property is speeded up, the falling property is also speeded up. Therefore, it is not possible to speed up the rising property and to slow down the falling property simultaneously. Namely, it is impossible to perform the speed up/down control of the rising property and the falling

property individually. According to a second means which the present invention takes, a method for switching on/off the switching element for selecting a charge element by a dedicated charge selecting control signal while switching on/off the switching element for selecting a discharge element by a dedicated charge selecting control signal is adopted. Thus, it becomes possible to set the optimal value of the rising property and the falling property respectively by controlling charge and discharge of the each switching circuit individually.

[Embodiment]

Next, an embodiment of the present invention is explained with reference to the attached drawings.

FIG. 1 is a block diagram showing an LCD driver integrated circuit which relates to the first embodiment of the present invention.

This LCD driver integrated circuit comprises a shift register 1 with n stages (for example a 64-bit) in which a serial data signal DIN is shifted to the next stage when a transfer clock CLK is inputted, a latch circuit array portion 2 in which a content of the each stage of the shift register 1 is taken in synchronization with an input of a latch signal LATCH and temporarily stored, a data selection portion 3 in which output portion control signals IN_1 to IN_{64} are generated based on an output of the each latch circuit and a condition input (an enable signal and the like), and an output transistor array portion 14 in which each of the LCDs (loads) connected to output terminals OUT_1 to OUT_{64} is charged and discharged based on the respective output control signals $IN_1$to IN_{64}.

The output transistor array portion 14 has switching portions 14_1 to 14_{64} which correspond to the respective LCDs in one-by-one relation and are controlled to switch

on/off by the output portion control signal IN_1 to IN_{64} and selecting control signals C_1 to C_{64} respectively. These selecting control signals C_1 to C_{64} are generated based on the revised data which is memorized in a memory portion 15 in advance.

FIG. 2 is a block diagram showing one of the switching portions. A switching portion 14_i is a parallel connected body of 8 tri-state buffer circuits 14_{i1} to 14_{i8} which are commonly inputted with an output portion control signal (a common control signal) IN_i and output to an output terminal OUT_i. As shown in FIG. 3, each of the tri-state buffer circuit 14_{i1} to 14_{i8} has MOSFET circuits having the same structure and connected in parallel to each other. For example, the tri-state buffer circuit 14_{i1} comprises a COMS inverter circuit having an N-Channel MOSFET 16a charge and a P-Channel MOSFET 16b discharge which are switched on/off exclusively by the output portion control signal IN_i, and an N-Channel MOSFET 17a for selecting a charge element and a P-Channel MOSFET 17b for selecting a discharge element which are switched on/off simultaneously by a selecting control signal C_{i1}. The selecting control signal C_{i1} is impressed to a gate of the P-Channel MOSFET 17b for selecting a discharge element through an inverter 18. The MOSFET 16a for charge is closed at H level of the output portion control signal IN_i to charge the output terminal OUT_i from a power source V_{DD}, and the MOSFET 17a for selecting a charge element is closed at H level of the selecting control signal C_{i1} to cut a bias of the power source V_{DD} to the MOSFET 16a for charge. In addition, the MOSFET 16b for discharge is closed at L level of the output portion control signal IN_i to discharge electricity of a load side to a ground side through the terminal OUT_i, and the MOSFET 17b for selecting a discharge element is closed at H level of the selecting control signal C_{i1} to cut the connection between the MOSFET 16b for discharge and a ground.

If 4 tri-state buffer circuits (for example 14_{i1} to 14_{i4}) among the switching portion 14_1 to 14_{64} are all selected, each output voltage waveform which comes up in the output terminal OUT1, OUT2, OUT3, and OUT4 is shown in FIG. 4, the rising property (a transmission time TPD1) of an output voltage of OUT1 and the falling property (a transmission time TPD3) are the standard value (normal value) respectively. Here, as for the switching portion 14_2, the rising time (a transmission time TPD2) is later than TPD1. Therefore, any one of the selecting control signals C_{25} to C_{28} is set at H level, and one or two or more among the other four MOSFET 17a for charge are closed to add a charge circuit in parallel, so that the falling property of the output voltage of the output terminal OUT2 becomes faster, and an on-voltage value is risen to be the same as the output voltage waveform of the output terminal OUT1. On the contrary, when the rising time of the output terminal OUT2 is too fast, one or two or more of the selecting control signals C_{21} to C_{24} are set at L level, and some of the charge circuits are reduced. In addition, as for a switching portion 14_4, the falling time (a transmission time TPD4) is later than TPD3. In this case, any one of the selecting control signals C_{45} to C_{48} is set at H level, and one or two or more among the other four MOSFETs 17b for discharge are closed to add a discharge circuit in parallel, so that the falling property of the output voltage of the output terminal OUT4 becomes later, and an off-voltage value is fallen to be the same as the output voltage waveform of the output terminal OUT3. On the contrary, when the falling time is too fast, one or two or more of the selecting control signals C_{41} to C_{44} are set at L level, and some of the discharge circuits are reduced.

However, although not shown in FIG. 4, when the falling time of the output voltage of OUT2 is made fast, the falling time becomes fast as well. That is, when any

one of the selecting control signals C_2 to C_{28} becomes H level, the MOSFET 17a for selecting a charge element and the MOSFET 17b for selecting a discharge element are closed simultaneously so that the rising time and the falling time are linked to each other. Due to a variation of an element property or the wiring length there are a switching portion of which the rising time is fast while the falling time is late or a switching portion which has a correlation opposite to this originally. Therefore, according to the above-described embodiment, it is not possible to completely revise the equalization of the transmission time or the on-voltage value.

FIG. 5 is a circuit diagram showing a structure of a switching portion which relates to the second embodiment of the present invention.

The different point of this circuit structure from that shown in FIG. 3 is that the selecting control signals C_{i1} to C_{i8} are directly applied to a gate of the MOSFET 17b each for selecting a discharge element, and the inverter 18 shown in FIG. 3 is removed. The MOSFET 17a for selecting a charge element is closed at H level of the selecting control signals C_{i1} to C_{i8} respectively whereas the MOSFET 17b for selecting a discharge element is closed at L level of the selecting control signals C_{i1} to C_{i8} respectively. That is, the MOSFET 17a for selecting a charge element and the MOSFET 17b for selecting a discharge element are switched on/off exclusively from each other by each of the selecting control signals C_{i1} to C_{i8}.

Here, the output voltage waveform each of the output terminals OUT1 to OUT4 is shown in FIG. 6, and the rising property and the falling property in the output voltage waveform of OUT1 corresponds to the standard value respectively. In the voltage waveform of the output terminal OUT2, the rising property and the falling property are both late. In such a case, during the charge period, one or two or more of

the selecting control signals C_{25} to C_{28} are set at H level, the number of closed MOSFETs 17a for selecting a charge element is increased, and a parallel charge circuit is added so that the rising property is made faster and the on-voltage value can be increased. In addition, during the discharge period, one of two or more of the selecting control signals C_{i5} to C_{i8} are changed to L level to increase the number of MOSFETs 17b for selecting a discharge element and add a discharge circuit in parallel, so that falling property is made faster and the off-voltage value can be decreased. Meanwhile, as for the output voltage waveform of the output terminal OUT3, although the rising property is late, the falling property nearly corresponds to the standard value. In such a case, it is enough to revise only the rising property. Thus, one or two or more of the selecting control signals C_{25} to C_{28} are set at H level during the charge period and during the discharge period, they are kept at H level to keep the control so as not to increase a discharge circuit. On the contrary, in the case that the rising property nearly corresponds to the standard value, whereas the falling property is late like the output voltage waveform of the output terminal OUT4, all the selecting control signals C_{45} to C_{48} are set at L level not to increase a charge circuit during the charge period, whereas during the discharge period one or two or more of the selecting control signals C_{45} to C_{48} are set at L level to increase a discharge circuit. Thus, by switching on/off the MOSFET 17a for selecting a charge element and the MOSFET 17b for selecting a discharge element by H/L of the selecting control signal exclusively each other, the co-movement of switching on/off therebetween, so that the speed up/down control of the rising property and the falling property can be performed individually. Note that the selecting control signal is required to be changed between high and low between the charge period and the discharge period, the timing control becomes slightly complex.

FIG. 7 is a block diagram showing an LCD driver circuit which relates to the third embodiment of the present invention. Note that in FIG. 7, in the same portion as a portion shown in FIG. 1 is denoted by the same reference and its explanation is omitted. This embodiment is improved one of the embodiment shown in FIG. 5, and an output transistor portion 24 comprises 2-control buffer circuits 24_1 to 24_{64}. A 2-control buffer circuit 24_i comprises 8 dedicated charge selecting control signals PC_{i1} to PC_{i8} (PC_i) and 8 dedicated discharge selecting control signals NC_{i1} to NC_{i8} (NC_i) as shown in FIG. 8. These control signals PC_i and NC_i are not changed between high and low between the charge period and the discharge period, and constantly keep a certain logic value level from start-up based on the revised data of the memory portion 15. Therefore, unlike the second embodiment, since it is not necessary to switch the level of the selecting control signal between the charge period and the discharge period, a timing control system can be simplified.

FIG. 9 is a block diagram showing an LCD driver circuit which relates to the fourth embodiment of the present invention. Note that in FIG. 9, in the same portion as a portion shown in FIG. 7 is denoted by the same reference and its explanation is omitted. An output transistor portion 4 of this embodiment is of the conventional structure, however, a buffer circuit portion 34 having the 2 control buffer circuits 24_1 to 24_{64} shown in FIG. 7 is provided between the data selecting portion 3 and the output transistor portion 4. The length of a wiring connecting each bit of the output transistor portion 4 to each bit of the data selecting portion 3 is different for each bit due to the layout, and thus, not only the rising property or the falling property is made fast or small but also that a signal delay inevitably arise. Provided that, as shown in FIG. 10, a waveform of a first bit output AIN_1 of the data selecting portion 3 is a standard value, an

output BIN_1 of the 2-control buffer circuit 24_1 is outputted without hardly delaying, and an illustrated waveform is appeared in the output terminal OUT1. Here, if a waveform of a second bit output AIN_2 of the data selecting portion 3 delays than that of the output AIN_1, by increasing a dedicated charge selecting control signal of the 2-control buffer circuit 24_2 and reducing the wiring resistance, a rising edge of an output BIN_2 of the 2-control buffer circuit 24_2 is hastened. Consequently, as for the output voltage waveform which appears in the output terminal OUT 2, not the falling property but the falling edge is hastened, and the falling property (inclination) is not changed. Obviously, it is possible to shift the falling edge of an output voltage.

[Effect of the Invention]

As explained above, the multi-output driver integrated circuit according to the present invention is characterized in that m switching circuits each in which is a switching means corresponding to a 1 bit output is connected in parallel is comprised, an element for selecting a charge element to cut a connection between an element for charge and a power source side and an element for selecting a discharge element to cut a connection between a switching element for charge and a ground side are provided in the each switching circuit, the both elements for selecting are controlled simultaneously or exclusively through a single or an independent control line, a parallel connection of a charge circuit or a discharge circuit is controlled to increase or decrease. Therefore, that brings the following effect.

(1) In the case where the element for selecting a charge element and the element for selecting a discharge element are controlled to switch on/off simultaneously by a single control line, it is possible to revise the transmission time and the on/off voltage value for

each output bit under the condition in that the rising property and the falling property of the output voltage waveform are linked to each other. In addition, the revision can be controlled by program, and therefore, it can be used as an interface circuit or a D-A converter.

(2) In the case where the element for selecting a charge element and the element for selecting a discharge element are controlled exclusively by a single control line or independently by a dedicated control line, even if there is any correlationship between the rising property and the falling property in a multi-bit, it is possible to correct with a high accuracy so as to correspond to the standard value and to effectively revise the variation of the transmission time and the on/off voltage. In addition, a delay time due to the difference of the wiring length (the wiring capacity) for each bit can be corrected.

4. Brief Description of the Drawings

FIG. 1 is a block diagram showing an LCD driver integrated circuit which relates to the first embodiment of the present invention.

FIG. 2 is a block diagram showing one switching portion in the above-mentioned embodiment.

FIG. 3 is a circuit diagram showing the detail of the above-mentioned switching portion.

FIG. 4 is a waveform diagram showing an example of revising the output voltage waveform in the same embodiment.

FIG. 5 is a circuit diagram showing the detail of a switching portion in the second embodiment of the present invention.

FIG. 6 is a waveform diagram showing an example of revising the output

voltage waveform in the same embodiment.

FIG. 7 is a block diagram showing an LCD driver integrated circuit which relates to the third embodiment of the present invention.

FIG. 8 is a circuit diagram showing one switching portion in detail in the same embodiment.

FIG. 9 is a block diagram showing an LCD driver integrated circuit which relates to the fourth embodiment of the present invention.

FIG. 10 is a waveform diagram showing an example of revising the output voltage waveform in the same embodiment.

FIG. 11 is a block diagram showing one example of a conventional LCD driver integrated circuit.

FIG. 12 (A), (B) is a circuit diagram each showing an output transistor portion in detail in the same conventional embodiment.

FIG. 13 is a waveform diagram showing a variation of an output voltage waveform between output bits in the same conventional embodiment.

[Explanation of the principal references]

1···shift register portion

2···latch circuit array portion

3···data selecting portion

14, 24···output transistor portion

14_1~14_{64}, 16_i···switching portion

14_{i1}~14_{i8}···tri-state buffer circuit

16a···MOSFET for charge

16b···MOSFET for discharge

17a···MOSFET for selecting a charge element

17b···MOSFET for selecting a discharge element

18···inverter

24_1~24_{64}, 24_i···2-control buffer circuit

34···buffer circuit portion

Patent Applicant: Fuji Electric Co., Ltd.

Agent: Patent attorney Minoru YAMADA